IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Hyoung-Joon Kim, Young-Wook Park, Byeong-Yun Nam

Serial No.: To Be Assigned Filed: Concurrently Herewith

For: METHODS OF FABRICATING INTEGRATED CIRCUIT DEVICES

PROVIDING IMPROVED SHORT PREVENTION

Date: November 12, 2003

Mail Stop PATENT APPLICATION Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Attached is a list of documents on form PTO-1449. Items 1-2 listed on the PTO-1449 were cited in parent application Serial No. 10/052,721, filed January 18, 2002. Since the benefit of this application is claimed under 35 U.S.C. §120, no copies need to be furnished in accordance with 37 C.F.R. §1.98(d); however, copies will be furnished on request. It is requested that these documents be considered by the Examiner and officially made of record in accordance with the provisions of 37 C.F.R. §1.56 and Section 609 of the MPEP.

No fee is believed due. However, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-0220.

Respectfully submitted,

Elizabeth A. Stanek Registration No. 48,568

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Form PTO-1449		U.S. Department of Commerce			Attorney Docket No. Serial No).	
		Patent and Trademark Office			5649-927DV To Be Assigned				
					Applicants:				
LIST OF DOCUMENTS CITED BY APPLICANT					Hyoung-Joon Kim, Young-Wook Park, Byeong-Yun Nam				
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		OTHER DO	OCUMENTS	(Includin	g Author, Title,	Date, Pertinent F	ages, Etc.)		
	2.	Klaus et al., Ator	nic Layer Dep	position of	SiO ₂ Using Catal	lyzed and Uncatal	vzed Self-Limiting	Surface	
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Examiner:	Date Considered:	

Examiner:

Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.